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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/548,414	04/13/2000	Takahiro Oguchi	P/1071-985	7261

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EXAMINER	
GARCIA, JOANNIE A	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/548,414	OGUCHI, TAKAHIRO	
	Examiner	Art Unit	
	Joannie A García	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,9,10 and 12-18* is/are pending in the application.

4a) Of the above claim(s) *5 and 13-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9,10,12 and 16-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20040526,20040803*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claims 2, 3, 9, 10, 12, and 16-18, are objected to because of the following informalities:

In claim 2, line 9, "and" after "support substrate;" should be deleted.

In claim 10, line 4, delete "a" before "semiconductor element substrate", and insert instead --the--.

In claim 14, line 3, delete "the" before "back surface side", and insert instead --a--.

In claim 16, line 8, delete "the" before "back surface side", and insert instead --a--.

Appropriate correction is required.

This application contains claims 5, and 13-15, drawn to an invention nonelected with traverse in Paper No. 01-17-02. A complete reply to the final rejection must include cancellation of nonelected claims or other appropriate action (37 CFR 1.144) See MPEP § 821.01.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3, 9, 10, 12, and 16-18, are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant's admitted prior art in combination with Franssila et al ("Etching through silicon wafer in inductively coupled plasma", Microsystems Technologies, April 2000 (2000-04), pp. 141-144, col. 6, no. 4).

Applicant's admitted prior art discloses manufacturing an external force detection sensor (Page 1, lines 9-11, and Page 4, lines 5-7) comprising providing a semiconductor element

substrate 3, providing a support substrate 2 (Figures 6A-6B, and 7C, Page 1, lines 12-18, and Page 4, lines 5-7), forming a recess 16 in a surface of the semiconductor element substrate (Figure 7A, and Page 4, lines 5-11), forming an etching stop layer 18 on a back surface of the semiconductor element substrate having the recess formed therein (Figure 7B, and Page 4, lines 5-7, and 13-17), through-hole dry etching the surface of the semiconductor element substrate using the etching stop layer (Figures 7C-7D, Page 4, lines 5-7, and 25-28, and Page 5, lines 1-2), joining a back surface side of said semiconductor element substrate with a surface of the support substrate having said recess formed therein (Figure 7C, and Page 4, lines 5-7, and 18-24), forming a sensor element including a vibrating body 5 (Figures 6B and 7D, Page 1, lines 19-23, Page 4, lines 5-7, and Page 5, lines 2-3), fixed electrodes 11 (Figures 6A-6B, and 7D-7E, Page 2, lines 10-14, Page 4, lines 5-7, and Page 5, lines 4-5), and movable electrodes 10 (Figure 6A-6B, and 7D-7E, Page 4, lines 5-7, and Page 5, line 5) on the semiconductor element substrate by dry etching (Page 4, lines 25-28, through Page 5, lines 1-7), removing the etching stop layer (Figure 7E, and Page 5, line 12), and completing the manufacturing of the external force detection sensor.

Applicant's admitted prior art discloses as well, manufacturing an external force detection sensor (Page 1, lines 9-11, and Page 4, lines 5-7) comprising forming a recessed part 16 on a back surface side 3b of a semiconductor silicon material element substrate 3 (Figures 6A-6B, and 7A, Page 1, lines 12-18, and Page 4, lines 5-11), wherein the recessed part is formed in a center portion of the back surface side of the semiconductor element substrate (Figure 7A, and Page 4, lines 5-11), forming a membrane 17 on a front surface side (Figure 7A, and Page 4, lines 8-12), providing an etching stop layer 18 on a top surface of the recessed part of said

semiconductor element substrate (Figure 7B, and Page 4, lines 5-7, and 13-17), anodically joining the back surface side of said semiconductor element substrate with a glass material support substrate 2 (Figure 7C, Page 1, lines 14-17, and Page 4, lines 5-7, and 18-24), and forming a sensor element including a vibrating body 5 (Figures 6B and 7D, Page 1, lines 19-23, Page 4, lines 5-7, and Page 5, lines 2-3), fixed electrodes 11 (Figures 6A-6B, and 7D-7E, Page 2, lines 10-14, Page 4, lines 5-7, and Page 5, lines 4-5), and movable electrodes 10 (Figure 6A-6B, and 7D-7E, Page 4, lines 5-7, and Page 5, line 5) on the semiconductor element substrate by dry etching (Page 4, lines 25-28, through Page 5, lines 1-7), removing the etching stop layer (Figures 7D-7E, Page 4, lines 5-7, and Page 5, lines 12-14), and completing the manufacturing of the external force detection sensor.

Applicant's admitted prior art discloses providing an etching stop layer 18 on a top surface of the recessed part of said semiconductor element substrate, wherein said etching stop layer is made of an oxide material using a CVD process (Figure 7B, and Page 4, lines 13-17). Applicant's admitted prior art does not teach providing said etching stop layer using an electrically conductive material such as aluminum, with an etch selectivity of not less than 1.

Franssila et al discloses through-hole etching silicon wafers required in the formation of sensor diaphragms, for example (Introduction, First Paragraph), using dielectric and/or metallic etching stop layers (Introduction, Fourth Paragraph), wherein using an oxide etching stop layer will show a severe notching effect, and using an aluminum etching stop layer will have no notching effect (Results and discussion, Sixth Paragraph). It would have been within the scope of one of ordinary skill in the art to combine the teachings of applicant's admitted prior art and

Franssila et al to enable the step of forming etching stop layer 18 of applicant's admitted prior art to be performed, by employing the either of the materials disclosed by Franssila et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joannie García whose telephone number is (571) 272-1861. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (571) 272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

George Fourson
Primary Examiner
Art Unit 2823

JAG
January 26, 2005

GFourson
Primary Examiner